AMENDMENTS TO THE SPECIFICATION

On page 5, please amend the paragraph beginning on line 22 and ending on line 24 as follows:

FIGS. 4C and 4D are [[is a]] top views of the connection of capacitor microstructures to each other and to non-active portions of a die using a microbridge brace layer according to the present invention.

Please amend the paragraph beginning on page 8, line 23, and ending on page 9, line 6, as follows:

The dielectric brace layer 390 usually will extend to other containers not shown in the figures so as to form a mechanical bracing support spanning between a considerable series of different containers along the common linkage of brace layer 390. Although a plurality of separate brace layers 390 can be used, it is also possible to provide more than one dielectric brace layer where they intersect at a container (or containers) such that a two-dimensional network or lattice of dielectric brace layers is formed through-out the array of containers (FIG. 4D). Also, the depth of the channels 39 formed that determines the thickness of the dielectric brace layer 390 is a function of the H/W container dimensions, the dielectric material used, and other factors. From a functional standpoint, the size of the dielectric brace layer must be selected to be large enough to provide lateral buttressing forces sufficient to substantially if not completely prevent the falling problems, yet not be so large that the relative weight of the brace layer becomes a factor. As to the width "w" of the brace layer 390, the brace generally has a width equal to or less than the largest cross-sectional dimension of the microstructures, which is the cylinder diameter "d" for the embodiment shown in FIG. 4A.

On page 9, please amend the paragraph beginning on line 13 and ending on line 27 as follows:

Referring to FIGS. 4C and 4D, each brace layer 390 not only connects a plurality of container capacitor microstructures 38 near their respective tops but it also ultimately extends to the edges of the IC die active circuit area 395, where the brace 390 locks to solid non-active portions 396 and 396' of a die 397 provided at the same elevation level as the brace layer 390. The non-active portions 396 and 396' of the die 397 are adjacent the fabricated circuitry 395. The brace layer 390 can extend linearly between the tops of capacitor microstructures 38 between non-active portions 396 and 396' of the die 397, or, as illustrated in FIGS. 4C and 4D, the brace layer 390 can follow a non-linear path before being anchored at its respective ends 390' and 390" at non-active areas 396 and 396' of the die 397. This provides an anchored system of braced-tall containers (or braced-tall stud capacitors according to a separate embodiment of this invention described in connection with FIG. 6E). In this way, the containers 38 are afforded good mechanical support in at least transverse or lateral directions to fortify the three-dimensional free-standing container microstructures to be defined during removing the second dielectric 36 and subjecting the in-process wafer to further handling and processing operations which are described below.